CLAIMS

What is claimed:

1. A method of dry plasma etching a semiconductor structure, having at least one semiconductor material layer, on a semiconductor wafer, comprising:
providing a dry plasma reaction gas mixture being chemically selected for, and having an etch rate corresponding to, each semiconductor material layer;
dividing the semiconductor structure into a masked portion and an unmasked portion; and
sequentially exposing the unmasked portion of the semiconductor structure to the dry plasma reaction gas mixture.

2. A method, as recited in Claim 1, wherein the dry plasma reaction gas mixture comprises methane gas and hydrogen gas.

3. A method, as recited in Claim 2, wherein the dry plasma reaction gas mixture comprises a gas volume ratio of one (1) part methane gas to four (4) parts hydrogen gas.

4. A method, as recited in Claim 2, wherein the dry plasma reaction gas mixture further comprises chlorine.

5. A method, as recited in Claim 4, wherein the dry plasma reaction gas mixture ratio comprises a combined methane gas and hydrogen gas mixture volume which is greater than that of the chlorine.

6. A method, as recited in Claim 5, wherein the dry plasma reaction gas mixture comprises a gas volume ratio of one (1) part methane gas to four (4) parts hydrogen gas to three (3) parts chlorine.

7. A method, as recited in Claim 1, wherein each at least one semiconductor material layer is distinct from one another.

8. A method, as recited in Claim 1;

wherein the step of providing the dry plasma reaction gas mixture comprises:

providing a first dry plasma reaction gas mixture;

providing a second dry plasma reaction gas mixture; and

providing a third dry plasma reaction gas mixture, and

wherein the etch rate of each subsequent dry plasma reaction gas mixture is greater than the etch rate of each previous dry plasma reaction gas mixture.

9. A method, as recited in Claim 1, wherein the step of sequentially exposing the unmasked portion of the semiconductor structure to the dry plasma reaction gas mixture comprises a technique selected from a group consisting essentially of:

(a) exposing the unmasked portion of the semiconductor structure to each given dry plasma reaction gas mixture such that each given subsequent semiconductor material layer acts as an etch-stop layer for each previous dry plasma reaction gas mixture; and

(b) exposing the unmasked portion of the semiconductor structure to the same given previous dry plasma reaction gas mixture such that a given subsequent semiconductor material layer is also etched.

10. A method, as recited in Claim 1, wherein the semiconductor wafer comprises a material selected from a group consisting essentially of gallium arsenide and indium phosphide.

11. A method, as recited in Claim 1, wherein the semiconductor material layer comprises a material selected from a group consisting essentially of indium gallium arsenide, gallium arsenide, indium aluminum arsenide, aluminum gallium arsenide, indium phosphide, indium gallium arsenic phosphide, and indium phosphide.

12. A method, as recited in Claim 1, wherein the sequentially exposing step comprises contemporaneously etching the at least one semiconductor material layer in situ.

13. A method, as recited in Claim 1, wherein the sequentially exposing step comprises using a temperature range of approximately 10°C to approximately 30°C.

14. A method, as recited in Claim 1, wherein the sequentially exposing step comprises using a negative bias power range of approximately 30 W to approximately 100 W.

15. A method, as recited in Claim 1, wherein the sequentially exposing step comprises using an inductively coupled power range of approximately 120 W to approximately 170 W.

16. A method, as recited in Claim 1, wherein the sequentially exposing step comprises using a pressure range of approximately 2 mTorr to approximately 7 mTorr.

17. A method, as recited in Claim 1, wherein the sequentially exposing step comprises:
analyzing the semiconductor structure for determining whether a desired vertical sidewall profile has been achieved; and
repeating the sequentially exposing step, if necessary, until the desired vertical sidewall profile has been achieved.

18. A method, as recited in Claim 7,
wherein the semiconductor structure comprises:
a first semiconductor material layer including indium gallium arsenide ($InGa_nAs_{1-n}$);
a second semiconductor material layer including indium aluminum arsenide ($InAl_nAs_{1-n}$); and
a third semiconductor material layer including indium phosphide (InP), and
wherein the sequentially exposing step is performed in situ and comprises:
initially exposing the first semiconductor material layer to a first dry plasma reaction gas mixture, comprising CH_4/H_2, wherein a reaction $InGa_nAs_{1-n} + CH_4/H_2 \rightarrow In(CH_3)_x\uparrow + Ga(CH_3)_x\uparrow + AsH_3\uparrow$ occurs, wherein n = a fraction in the range of approximately 0.3 to approximately 0.6 and x = an integer such as 1, 2, or 3, and whereby resultant species are volatilized;
subsequently exposing the second semiconductor layer to a second reaction gas mixture, comprising $CH_4/H_2/Cl_2$, wherein a reaction $InAl_nAs_{1-n}$ +

$CH_4/H_2/Cl_2$ –> $In(CH_3)_x\uparrow$ + $As(CH_3)_x\uparrow$ + $AlCl_3\uparrow$ occurs, wherein n = a fraction in the range of approximately 0.3 to approximately 0.6 and x = an integer such as 1, 2, or 3, and whereby resultant species are volatilized; and

finally exposing the third semiconductor layer to the same second reaction gas mixture, wherein a reaction InP + $CH_4/H_2/Cl_2$ –> $In(CH_3)_x\uparrow$ + $PH_3\uparrow$ occurs, wherein x = an integer such as 1, 2, or 3, and whereby resultant species are volatilized.

19. A method of dry plasma etching a semiconductor structure, having at least one semiconductor material layer, on a semiconductor wafer, comprising:

providing a dry plasma reaction gas mixture being chemically selected for, and having an etch rate corresponding to, each semiconductor material layer;

dividing the semiconductor structure into a masked portion and an unmasked portion; and

sequentially exposing the unmasked portion of the semiconductor structure to the dry plasma reaction gas mixture,

wherein an initial dry plasma reaction gas mixture comprises methane gas and hydrogen gas, and

wherein a subsequent dry plasma reaction gas mixture comprises methane gas, hydrogen gas, and chlorine.

20. A method of dry plasma etching a semiconductor structure, having at least one semiconductor material layer, on a semiconductor wafer, comprising:

providing a dry plasma reaction gas mixture being chemically selected for, and having an etch rate corresponding to, each semiconductor material layer;

dividing the semiconductor structure into a masked portion and an unmasked portion; and

sequentially exposing the unmasked portion of the semiconductor structure to the dry plasma reaction gas mixture,

wherein the at least one semiconductor material layer comprises a material selected from a group consisting essentially of indium gallium arsenide, gallium arsenide, indium aluminum arsenide, aluminum gallium arsenide, indium phosphide, indium gallium arsenic phosphide, and indium phosphide.